WHAT IS CLAIMED IS:

1. A semiconductor device test circuit for testing a functional macro circuit, the circuit comprising:

a plurality of first flip-flop circuits connected in series so that serial test pattern data latched at a stage will be latched at the next stage in synchronization with a first clock signal; and

a plurality of second flip-flop circuits for outputting the test pattern data latched by the plurality of first flip-flop circuits to the functional macro circuit in synchronization with a second clock signal.

2. The semiconductor device test circuit according to claim 1, wherein the plurality of first flip-flop circuits and the plurality of second flip-flop circuits are delayed flip-flop circuits.

3. The semiconductor device test circuit according to claim 1, further comprising selector circuits for selecting the test pattern data outputted from each of the plurality of second flip-flop circuits or a signal from a user logic and outputting the selected test pattern data or the selected signal to the functional macro circuit in accordance with a control signal.

4. The semiconductor device test circuit according to claim 1, further comprising, a circuit including a selector circuit and a third flip-flop circuit, wherein a signal outputted

from the functional macro circuit and the test pattern data outputted from the first flip-flop circuit at a last stage are inputted to the selector circuit at a first stage, while a signal outputted from the functional macro circuit and a signal outputted from the third flip-flop circuit at a preceding stage are inputted to the selector circuit at each of subsequent stages, further wherein the third flip-flop circuit latches a signal selected by the selector circuit in synchronization with the first clock signal.

5. The semiconductor device test circuit according to claim 4, wherein the third flip-flop circuit is a delayed flip-flop circuit.

6. The semiconductor device test circuit according to claim 4, wherein the third flip-flop circuit included in the circuit at a last stage serially outputs the test pattern data or the signal outputted from the functional macro circuit.

7. A semiconductor device comprising:

a plurality of functional macro circuits;

a plurality of semiconductor device test circuits each including:

a plurality of first flip-flop circuits connected in series so that serial test pattern data latched at a stage will be latched at the next stage in synchronization with a first clock signal, and

a plurality of second flip-flop circuits for outputting the test pattern data latched by the plurality of first flip-flop circuits to the corresponding functional macro circuit in synchronization with a second clock signal;

a plurality of third flip-flop circuits, the number of the plurality of third flip-flop circuits depending on the number of the plurality of semiconductor device test circuits, connected in series for outputting a control signal for specifying one of the plurality of semiconductor device test circuits in synchronization with a third clock signal;

a first selector circuit for selecting one of the plurality of semiconductor device test circuits to which the first clock signal is to be inputted in accordance with the control signal;

a second selector circuit for selecting one of the plurality of semiconductor device test circuits to which the second clock signal is to be inputted in accordance with the control signal; and

a third selector circuit for selecting one of signals outputted from the plurality of semiconductor device test circuits in accordance with the control signal.

8. The semiconductor device according to claim 7, wherein the signal for specifying the semiconductor device test circuit is inputted from a test data input terminal where the test pattern data is inputted to the third flip-flop circuit at a first stage.